IN THE CLAIMS

1. (Currently Amended) A method comprising:

preparing a substrate with only PWELLs; and

forming one or more dual gate structures including NWELLS in the substrate using only one mask.

2. (Original) The method of claim 1, wherein preparing a substrate comprises:

forming a sacrificial oxide layer on a semiconductor.

3. (Currently Amended) The method of claim 1, wherein preparing a substrate with only PWELLS comprises:

forming a gate oxide layer on a semiconductor with only PWELLs; and

forming a polysilicon layer on the gate oxide layer.

4. (Original) The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises:

forming a first gate structure having a first conductivity in the substrate, the first gate structure being formed using one or more blanket implants; and

forming a second gate structure having a second conductivity in the substrate, the second conductivity having a different value than the first conductivity and the second gate structure being formed using only one masking operation.

5. (Original) A method comprising:

preparing a substrate;

forming a first gate structure including a PWELL without using a mask; and

forming a second gate structure including an NWELL using only one mask.

6. (Original) The method of claim 5, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL.

7. - 8. (Canceled)

9. (Original) A method comprising:

preparing a substrate;

forming a first gate structure including a PWELL having a depth of about 200 nanometers without using a mask; and

forming a second gate structure including an NWELL using only one mask.

10. (Original) The method of claim 9, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL.

11. - 35. (Canceled)

36. (Previously Presented) A method of forming one or more dual gate structures, the method comprising:

forming one or more gate structures including a PWELL without a mask;

masking one or more PWELL regions; and

forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

37. (Canceled)

38. (Previously Presented) A method of forming one or more dual gate structures, the method comprising:

forming one or more gate structures including a PWELL using blanket implants;

masking one or more PWELL regions; and

forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

39.-44. (Canceled)

45. (Previously Presented) The method of claim 1, preparing the substrate comprises forming a PWELL in an n-type substrate.

46. (Previously Presented) The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises forming one or more complementary metal-oxide semiconductor dual gate structures in the substrate using only one mask.

47. (Previously Presented) The method of claim 2, wherein forming the sacrificial oxide layer on the semiconductor comprises growing a sacrificial oxide layer to a depth of a few microns.

48. (Previously Presented) The method of claim 3, wherein forming the gate oxide layer on the semiconductor comprises forming the gate oxide layer having a thickness of between about five nanometers and about ten nanometers.

49. (Previously Presented) The method of claim 5, wherein preparing the substrate comprises forming a PWELL in an n-type substrate.

50. (Previously Presented) The method of claim 5, wherein forming the first gate structure including the PWELL without using the mask comprises forming the PWELL by a blanket implant of boron ions at about 430 keV.

51. (Previously Presented) The method of claim 5, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a depth of about 200 nanometers.

52. (Previously Presented) The method of claim 5, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a blanket implant of boron ions at about 430 keV and a depth of about 200 nanometers.

53. (Previously Presented) The method of claim 49, wherein forming the first gate structure including the PWELL without using the mask comprises forming the PWELL by a blanket implant of boron ions at about 430 keV.

54. (Previously Presented) The method of claim 49, wherein forming the first gate structure including the PWELL without using the masking comprises forming the PWELL having a depth of about 200 nanometers.

55. (Previously Presented) The method of claim 9, wherein preparing the substrate comprises forming a PWELL in an n-type substrate.

56. (Canceled)

57. (New) A method comprising:

preparing a substrate with only NWELLs; and

forming one or more dual gate structures including PWELLS in the substrate using only one mask.

58. (New) The method of claim 57, wherein preparing a substrate with only NWELLs comprises:

forming a sacrificial oxide layer on a semiconductor.

59. (New) The method of claim 57, wherein preparing a substrate with only NWELLs comprises:

forming a gate oxide layer on a semiconductor with only NWELLs; and

forming a polysilicon layer on the gate oxide layer.